IN THE CLAIMS:

1-75. (Cancelled)

76. (New) A media processing apparatus which inputs a data stream including compressed audio data and compressed video data, decodes data in the inputted data stream, and respectively outputs the decoded audio data and the decoded video data to an external display device and an external audio output device, the media processing apparatus comprising:

an input/output processing unit operable to perform an input/output processing, asynchronously occurring due to an external factor,

wherein the input/output processing unit is composed of:

an input unit operable to input an asynchronous data stream;

a video output unit operable to output the decoded video data to the external display device;

an audio output unit operable to output the decoded audio data to the external audio output device; and

a processor for executing task programs from a first task program through a fourth task program stored in an instruction memory, by switching between the respective four task programs, the task programs including:

the first task program for transferring the data stream from the input unit to the memory;

the second task program for supplying the data stream from the memory to a decode processing unit;

the third task program for outputting the decoded video data from the memory to the video output unit; and

the fourth task program for outputting the decoded audio data from the memory to the audio output unit,

the media processing apparatus further comprising:

the decode processing unit operable, in parallel with the input/output processing, to perform a decode processing where decoding of the data stream stored in the memory is mainly performed,

wherein the decoded video data and the decoded audio data are stored in the memory.

77. (New) The media processing apparatus of Claim 76, herein the processor is composed of:

a program counter unit including at least four program counters corresponding to the task programs from the first task program to the fourth task program;

an instruction fetch unit for fetching an instruction from the instruction memory which stores the task programs, using an instruction address designated by one of the program counters;

an instruction execution unit for executing the instruction fetched by the instruction fetch unit; and

a task control unit for controlling the instruction fetch unit to sequentially switch the program counter every time a predetermined number of instruction cycles have elapsed.

78. (New) The media processing apparatus of Claim 77, wherein the processor is further composed of

a register unit including at least four register sets corresponding to the program tasks from the first task program to the fourth task program, and

wherein the task control unit, simultaneously with switching of a program counter, switches a present register set to a register set which is to be used by the instruction execution unit.

79. (New) The media processing apparatus of Claim 78 wherein the task control unit is composed of:

a counter for counting a number of instruction cycles in accordance with a clock signal every time the program counter is switched; and

a switch instruction unit for controlling the instruction fetch unit to switch the program counter when a count value of the counter reaches the predetermined number.

80. (New) The media processing apparatus of Claim 79, wherein the decode processing unit is composed of: a sequential processing unit operable to perform a sequential processing, which is mainly for condition judgments, on the data in the data stream, the sequential processing including a header analysis of the compressed audio data and the compressed video data and a decoding of the compressed audio data; and

a routine processing unit operable to perform a routine processing in parallel with the sequential processing, the routine processing including a decoding of the compressed video data except for the header analysis.

81. (New) The media processing apparatus of Claim 80,

wherein the sequential processing unit alternates between performing a header analysis for analyzing a header which is assigned to a predetermined unit of data (hereinafter, called a "block") in the data stream and performing a decoding of the compressed audio data in the data stream, instructs the routine processing unit to decode a block when the header analysis for the block is completed, and starts the header analysis of a next block when receiving notification from the routine processing unit that the decoding of the block is completed; and

wherein the routine processing unit decodes the compressed video data for a block in accordance with a result of the header analysis given by the sequential processing unit.

82. (New) The media processing apparatus of Claim 81, wherein the routine processing unit is composed of:

a data translation unit operable to perform variable length code decoding (abbreviated as the "VLD" hereafter) on the compressed video data of the data stream in accordance with an instruction from the sequential processing unit;

a calculation unit operable to perform inverse quantization (abbreviated as the "IQ" hereafter) and inverse discrete cosine transformation (abbreviated as the "IDCT" hereafter) by executing a predetermined calculation on a video block obtained through the VLD; and

a blending unit operable to restore video block data which corresponds to the video block by blending a decoded rectangular image of a frame stored in the memory with the video block data on which the IDCT has been performed.

83. (New) The media processing apparatus of Claim 82, wherein the calculation unit includes

a first buffer having a storage area whose capacity is equivalent to one block, and

wherein the data translation unit includes:

a VLD unit operable to perform the VLD on the compressed video data of the data stream;

a first address table unit operable to store a first address sequence where addresses in the first buffer are arranged in an order for a zigzag scan;

a second address table unit operable to store a second address sequence where addresses in the first buffer are arranged in an order for an alternate scan; and

a writing unit operable to write block data obtained through the VLD performed by the VLD unit into the first buffer in accordance with one of the first address sequence and the second address-sequence.

84. (New) The media processing apparatus of Claim 83, wherein the writing unit includes:

a table address generate unit operable to sequentially generate a table address for the first address table unit and the second address table unit;

an address select unit operable to sequentially select one of an address of the first address sequence and an address of the second address sequence which are separately outputted from the first table unit and the second table unit into which the table address has been inputted; and

an address output unit operable to sequentially output the selected address to the first buffer.

85. (New) A media processing apparatus comprising:

an input unit operable to input a data stream including compressed audio data and compressed video data;

a sequential processing unit operable to perform a sequential processing which is mainly for condition judgments, the sequential processing including performing a header analysis for analyzing a header which is assigned to a predetermined unit of data (hereinafter called a "block") in the data stream and performing a decoding of compressed audio data of the data stream; and

a routine processing unit operable to perform, in parallel with the sequential processing, a routine processing which is mainly for routine calculations, the routine processing including a decoding of the compressed video data of the data stream for a block using a result of the header analysis,

wherein the routine processing unit is composed of:

a data translation unit operable to perform variable length code decoding (abbreviated as the "VLD" hereafter) on the compressed video data of the data stream in accordance with an instruction from the sequential processing unit;

a calculation unit operable to perform inverse quantization (abbreviated as the "IQ" hereafter) and inverse discrete cosine transformation (abbreviated as the "IDCT" hereafter) by executing a predetermined calculation on a video block obtained through the VLD; and

a blending unit operable to restore video block data by performing motion compensation processing which is achieved by blending the decoded block with the video block on which the IDCT has been performed, and

wherein the sequential processing unit is composed of:

an obtaining unit operable to obtain header information on which the VLD has been performed by the data translation unit;

an analyzing unit operable to analyze the obtained header information;

a notifying unit operable to report parameters obtained as a result of the header analysis to the routine processing unit;

an audio decoding unit operable to decode the compressed audio data of the data stream inputted by the input unit; and

a control unit operable to stop an operation of the audio decoding unit and activating the obtaining unit that indicates a decode completion of the block, and for instructing the data translation unit to start the VLD on the compressed video data of the data stream when the parameters have been indicated by the notifying unit.

86. (New) The media processing apparatus of Claim 85, wherein the analyzing unit calculates a quantization scale and a motion vector in accordance with the header information, and

wherein the notifying unit notifies the calculation unit of the quantization scale and notifies the blending unit of the motion vector.

87. (New) The media processing apparatus of Claim 86, wherein the calculation unit is composed of:

a first control storage unit and a second control storage unit which each store a microprogram;

a first program counter for designating a first read address to the first control storage unit;

a second program counter for designating a second read address:

a selector for selecting one of the first read address and the second read address and outputting the selected read address to the second control storage unit; and

an execution unit, which includes a multiplier and an adder, for executing the IQ and IDCT in block units according to microprogram control by the first control storage unit and the second control storage unit.

88. (New) The media processing apparatus of Claim 87, wherein the execution unit separately performs a processing using the multiplier and a processing using the adder in parallel when the second read address is selected by the selector, and performs the processing using the multiplier and the processing using the adder in coordination when the first read address is selected by the selector.

89. (New) The media processing apparatus of Claim 88, wherein the calculation unit is further composed of:

a first buffer for holding a video block inputted from the data translation unit; and

a second buffer for holding a video block on which the IDCT has been performed by the execution unit, and

wherein the first control storage unit stores a microprogram for the IQ and a microprogram for the IDCT, wherein the second control storage unit stores a microprogram for the IDCT and a microprogram for transferring a video block on which the IDCT has been performed to the second buffer, and

wherein the execution unit executes a processing to transfer the video block on which the IDCT has been performed to the second buffer and the IQ processing of a next video block in parallel, and executes the IDCT processing of the next video block, on which the IQ processing has been performed, using the multiplier and the adder in coordination.

90. (New) The media processing apparatus of Claim 89, wherein the blending unit further generates a differential block representing a differential image from video data which is to be compressed;

wherein the second buffer stores the generated differential block,

wherein the first control storage unit further stores a microprogram for discrete cosine transformation (abbreviated as the "DCT" hereafter) and a microprogram for quantization processing (abbreviated as the "Q processing" hereafter), wherein the second control storage unit further stores a microprogram for the DCT and a microprogram for transferring the video block on which the DCT has been performed to the first buffer,

wherein the execution unit further executes the DCT and Q processing on the differential block stored in the second buffer and transfers the differential block on which the DCT and Q processing has been performed to the first buffer,

wherein the data translation unit further performs variable length coding (abbreviated as the "VLC" hereafter) on the block stored in the first buffer, and

wherein the sequential processing unit further assigns header information to a block on which the VLD has been performed by the data translation unit.

91. (New) The media processing apparatus of Claim 87, wherein the input unit further inputs polygon data, wherein the sequential processing unit further analyzes the polygon data and calculates vertex coordinates and edge inclinations of the polygon, and

wherein the routine processing unit further generates image data of the polygon in accordance with the calculated vertex coordinates and edge inclinations.

92. (New) The media processing apparatus of Claim 91, wherein the first control storage unit and the second control storage unit each store a microprogram for performing a scan conversion based on a digital differential analyze algorithm, and

wherein the execution unit performs the scan conversion based on the vertex coordinates and edge inclinations calculated by the sequential processing unit according to control of the microprogram.

93. (New) The media processing apparatus of Claim 86, wherein the calculation unit is composed of:

a first control storage unit and the second control storage unit for respectively storing a microprogram;

a first program counter for designating a first read address to the first control storage unit;

a second program counter for designating a second read address;

a selector for selecting one of the first read address and the second read address and outputting the selected address to the second control storage unit; and

a plurality of execution units for executing the IQ and IDCT in units of blocks according to control of the microprogram by the first control storage unit and the second control storage unit, each execution unit including a multiplier and an adder, and

wherein each execution unit takes charge of a partial block which is divided from the block.

94. (New) The media processing apparatus of Claim 93, wherein the calculation unit is further composed of:

a plurality of address translation tables which are set corresponding to the plurality of execution units, each address translation table storing translated addresses whose order is partially changed in a predetermined address sequence;

an instruction register group including a plurality of registers which each store a microinstruction associated with one of the translated addresses, each microinstruction forming part of a microprogram that realizes a predetermined calculation; and

a switching unit, which is set between the first and second control storage units and the plurality of execution units, for outputting microinstructions from the instruction registers to the plurality of execution units in place of a microinstruction outputted from one of the first control storage unit and the selector to every execution unit, and

wherein when the first read address or the second read address is an address of the predetermined address sequence, the address is translated into the translated addresses by the address translation tables, and

wherein the instruction register group outputs the microinstructions corresponding to the translated addresses outputted from the address translation tables.

95. (New) The media processing apparatus of Claim 94, wherein

when a microinstruction indicating one of an addition or subtraction operation is outputted from one of the instruction registers, each address translation table outputs a flag showing whether the microinstruction indicates an addition or a subtraction while the first program counter is outputting the first read address in the predetermined address sequence,

the plurality of execution units perform addition or subtraction in accordance with the flag, and

the flag is set in accordance with the microinstruction of the second control storage unit.

96. (New) The media processing apparatus of Claim 94,

wherein the second control storage unit further outputs information showing a storage destination of a microinstruction execution result at a same time of an output of the microinstruction stored in the register while the first program counter outputs the first read address of the predetermined address sequence, and

wherein each execution unit stores the execution result in accordance with the storage destination information.

97. (New) A media processing apparatus which inputs a data stream including compressed audio/video (AV) data, decodes the inputted stream data, and outputs the decoded data, the media processing apparatus comprising:

an input/output processing unit operable to perform input/output processing in which a plurality of input/output-related tasks, including a task for storing a data stream asynchronously inputted due to an external factor in a memory, are executed, the plurality of input/output-related tasks being switched at predetermined intervals;

a sequential processing unit operable to perform a sequential processing mainly for condition judgments, the sequential processing including a header analysis of the compressed audio data and the compressed video data and a decoding of the compressed audio data, whereby the decoded audio data is stored in the memory; and

a routine processing unit operable to perform a routine processing mainly for routine calculations on the compressed video data stored in the memory in accordance with a result of the header analysis given by the sequential processing unit, the routine processing including a decoding of the compressed video data, whereby the decoded video data is stored in the memory, and

wherein the plurality of input/output-related tasks further include a task for reading the decoded audio data and the decoded video data from the memory and respectively outputting the read audio data and the read video data,

wherein the header analysis is a header analysis of a macroblock including a plurality of video blocks.

98. (New) The media processing apparatus of Claim 97,

wherein the sequential processing unit alternates between performing a header analysis for analyzing a header which is assigned to a predetermined unit of data (hereinafter, called a "block") in the data stream and performing a decoding of the compressed audio data in the data stream, instructs the routine processing unit to decode a block when the header analysis for the block is completed, and starts the header analysis of a next block when receiving notification from the routine processing unit that the decoding of the block is completed; and

wherein the routine processing unit decodes the compressed video data for a block in accordance with a result of the header analysis given by the sequential processing unit.

99. (New) The media processing apparatus of Claim 98, wherein the routine processing unit is composed of:

a data translation unit operable to perform variable length code decoding (abbreviated as the "VLD" hereafter) on the compressed video data of the data stream in accordance with an instruction from the sequential processing unit;

a calculation unit operable to perform inverse quantization (abbreviated as the "IQ" hereafter) and inverse discrete cosine transformation (abbreviated as the "IDCT" hereafter) by executing a predetermined calculation on a video block obtained through the VLD; and

a blending unit operable to restore video block data which corresponds to the video block by blending a decoded rectangular image of a frame stored in the memory with the video block data on which the IDCT has been performed.

100. (New) The media processing apparatus of Claim 99, wherein the calculation unit includes:

a first buffer having a storage area whose capacity is equivalent to one block, and

wherein the data translation unit includes:

a VLD unit for performing the VLD on the compressed video data of the data stream;

a first address table unit operable to store a first address sequence where addresses in the first buffer are arranged in an order for a zigzag scan;

a second address table unit operable to store a second address sequence where addresses in the first buffer are arranged in an order for an alternate scan; and

a writing unit operable to write block data obtained through the VLD performed by the VLD unit into the first buffer in accordance with one of the first address sequence and at the second address sequence.

101. (New) The media processing apparatus of Claim 100, wherein the writing unit includes:

a table address generate unit operable to sequentially generate a table address for the first address table unit and the second address table unit;

an address select unit operable to sequentially select one of an address of the first address sequence and an address of the second address sequence which are separately outputted from the first table unit and the second table unit into which the table address has been inputted; and

an address output unit operable to output the selected address to the first buffer.

102. (New) The media processing apparatus of Claim 97,

wherein the input/output processing unit is composed of:

an input unit operable to input an asynchronous data stream;

a video output unit operable to output the decoded video data to the external display device;

an audio output unit operable to output the decoded audio data to the external audio output device; and

a processor for executing task programs from a first task program to a fourth task program stored in an instruction memory, by switching between the four task programs, the task programs including:

the first task program for transferring the data stream from the input unit to the memory;

the second task program for supplying the data stream from the memory to the decode processing unit;

the third task program for outputting the decoded video data from the memory to the video output unit; and

the fourth task program for outputting the decoded audio data from the memory to the audio output unit,

wherein the first, second, third, and fourth tasks are the plurality of input-output-related tasks.

103. (New) The media processing apparatus of Claim 102, wherein the processor is composed of:

a program counter unit including at least four program counters corresponding to the task programs from the first task program to the fourth task program;

an instruction fetch unit for fetching an instruction from the instruction memory which stores the task programs, using an instruction address designated by one of the program counters;

an instruction execution unit for executing the instruction fetched by the instruction fetch unit; and

a task control unit for controlling the instruction fetch unit to sequentially switch the program counter every time a predetermined number of instruction cycles have elapsed.

104. (New) The media processing apparatus of Claim 103,

wherein the processor is further composed of

a register unit including at least four register sets corresponding to the program tasks from the first task program to the fourth task program, and

wherein the task control unit, simultaneously with switching of a program counter, switches a present register set to a register set which is to be used by the instruction execution unit.

105. (New) The media processing apparatus of Claim 104, wherein the task control unit is composed of:

a counter for counting a number of instruction cycles in accordance with a clock signal every time the program counter is switched; and

a switch instruction unit for controlling the instruction fetch unit to switch the program counter when a count value of the counter reaches the predetermined number.

106. (New) The media processing apparatus of Claim 104,

wherein the routine processing unit is composed of:

a data translation unit operable to perform variable length code decoding (abbreviated as the "VLD" hereafter) on the compressed video data of the data stream in accordance with an instruction from the sequential processing unit;

a calculation unit operable to perform inverse quantization (abbreviated as the "IQ" hereafter) and inverse discrete cosine transformation (abbreviated as the "IDCT" hereafter) by executing a predetermined calculation on a video block obtained through the VLD; and

a blending unit operable to restore video block data which corresponds to the video block by blending a decoded rectangular image of a frame stored in the memory with the video block data on which the IDCT has been performed.

107. (New) The media processing apparatus of Claim 106, wherein the analyzing unit calculates a quantization

scale and a motion vector in accordance with the header information, and

wherein the notifying unit notifies the calculation unit of the quantization scale and notifies the blending unit of the motion vector.

108. (New) The media processing apparatus of Claim 107, wherein the calculation unit is composed of:

a first control storage unit and a second control storage unit which each store a microprogram;

a first program counter for designating a first read address to the first control storage unit;

a second program counter for designating a second read address;

a selector for selecting one of the first read address and the second read address and outputting the selected read address to the second control storage unit; and

an execution unit, which includes a multiplier and an adder, for executing the IQ and IDCT in block units according to microprogram control by the first control storage unit and the second control storage unit.

109. (New) The media processing apparatus of Claim 108,

wherein the execution unit separately performs a processing using the multiplier and a processing using the adder in parallel when the second read address is selected by the selector, and performs the processing using the multiplier and the processing using the adder in coordination when the first read address is selected by the selector.

110. (New) The media processing apparatus of Claim 109,

wherein the calculation unit is further composed of a first buffer for holding a video block inputted from the data translation unit; and

a second buffer for holding a video block on which the IDCT has been performed by the execution unit, and

wherein the first control storage unit stores a microprogram for the IQ and a microprogram for the IDCT, wherein the second control storage unit stores a microprogram for the IDCT and a microprogram for transferring a video block on which the IDCT has been performed to the second buffer, and

wherein the execution unit executes a processing to transfer the video block on which the IDCT has been performed to the second buffer and the IQ processing of a next video block in parallel, and executes the IDCT processing of the next video block, on which the IQ processing has been performed, using the multiplier and the adder, in coordination.

111. (New) The media processing apparatus of Claim 110,

wherein the blending unit further generates a differential block representing a differential image from video data which is to be compressed;

wherein the second buffer stores the generated differential block,

wherein the first control storage unit further stores a microprogram for discrete cosine transformation (abbreviated as the "DCT" hereafter) and a microprogram for quantization processing (abbreviated as the "Q processing" hereafter),

wherein the second control storage unit further stores a microprogram for the DCT and a microprogram for transferring the video block on which the DCT has been performed to the first buffer,

wherein the execution unit further executes the DCT and Q processing on the differential block stored in the second buffer and transfers the differential block on which the DCT and Q processing has been performed to the first buffer,

wherein the data translation unit further performs variable length coding (abbreviated as the "VLC" hereafter) on the block stored in the first buffer, and

wherein the sequential processing unit further assigns header information to a block on which the VLD has been performed by the data translation unit.

112. (New) The media processing apparatus of Claim 107, wherein the calculation unit is composed of:

a first control storage unit and the second control storage unit for respectively storing a microprogram;

a first program counter for designating a first read address to the first control storage unit;

a second program counter for designating a second read address;

a selector for selecting one of the first read address and the second read address and outputting the selected address to the second control storage unit; and

a plurality of execution units for executing the IQ and IDCT in units of blocks according to control of the microprogram by the first control storage unit and the second control storage unit, each execution unit including a multiplier and an adder, and

wherein each execution unit takes charge of a partial block which is divided from the block.

113. (New) The media processing apparatus of Claim 112, wherein the calculation unit is further composed of:

a plurality of address translation tables which are set corresponding to the plurality of execution units, each address translation table storing translated addresses whose order is partially changed in a predetermined address sequence;

an instruction register group including a plurality of registers which each store a microinstruction associated with one of the translated addresses, each microinstruction forming part of a microprogram that realizes a predetermined calculation; and

a switching unit, which is set between the first and second control storage units and the plurality of execution units, for outputting microinstructions from the instruction registers to the plurality of execution units in place of a microinstruction outputted from one of the first control storage unit and the selector to every execution unit, and

wherein when the first read address or the second read address is an address of the predetermined address sequence, the address is translated into the translated addresses by the address translation tables, and

wherein the instruction register group outputs the microinstructions corresponding to the translated addresses outputted from the address translation tables.

114. (New) The media processing apparatus of Claim 113, wherein

when a microinstruction indicating one of an addition or subtraction operation is outputted from one of the instruction registers, each address translation table outputs a flag showing whether the microinstruction indicates an addition or a subtraction while the first program counter is outputting the first read address in the predetermined address sequence,

the plurality of execution units perform addition or subtraction in accordance with the flag, and

the flag is set in accordance with the microinstruction of the second control storage unit.

115. (New) The media processing apparatus of Claim 113,

wherein the second control storage unit further outputs information showing a storage destination of a microinstruction execution result at a same time of an output of the microinstruction stored in the register while the first program counter outputs the first read address of the predetermined address sequence, and

wherein each execution unit stores the execution result in accordance with the storage destination information.

116. (New) The media processing apparatus of Claim 106,

wherein the calculation unit includes

a first buffer having a storage area whose capacity is equivalent to one block, and

wherein the data translation unit includes:

a VLD unit operable to perform the VLD on the compressed video data of the data stream;

a first address table unit operable to store a first address sequence where addresses in the first buffer are arranged in an order for a zigzag scan;

a second address table unit operable to store, second address sequence where addresses in the first buffer are arranged in an order for an alternate scan; and

a writing unit operable to write block data obtained through the VLD performed by the VLD unit, into the first buffer in accordance with one of the first address sequence and the second address sequence.

117. (New) The media processing apparatus of Claim 116, wherein the writing unit includes:

a table address generate unit operable to sequentially generate a table address for the first address table unit and the second address table unit;

an address select unit operable to sequentially select one of an address of the first address sequence and an address of the second address sequence which are separately outputted from the first table unit and the second table unit into which the table address has been inputted; and

an address output unit operable to output the selected address to the first buffer.

118. (New) The media processing apparatus of Claim 117,

wherein the analyzing unit operable to calculate a quantization scale and a motion vector in accordance with the header information, and

wherein the notifying unit notifies the calculation unit of the quantization scale and notifies the blending unit of the motion vector.

119. (New) The media processing apparatus of Claim 118, wherein the calculation unit is composed of:

a first control storage unit and a second control storage unit which each store a microprogram;

a first program counter for designating a first read address to the first control storage unit;

a second program counter for designating a second read address;

a selector for selecting one of the first read address and the second read address and outputting the selected read address to the second control storage unit; and

an execution unit, which includes a multiplier and an adder, for executing the IQ and IDCT in block units according to microprogram control by the first control storage unit and the second control storage unit.

120. (New) The media processing apparatus of Claim 119,

wherein the execution unit separately performs a processing using the multiplier and a processing using the adder in parallel when the second read address is selected by the selector, and performs the processing using the multiplier and the processing using the adder in coordination when the first read address is selected by the selector.

121. (New) The media processing apparatus of Claim 120,

wherein the calculation unit is further composed of

a second buffer for holding a video block on which the IDCT has been performed by the execution unit, and.

wherein the first control storage unit stores a microprogram for the IQ and a microprogram for the IDCT, wherein the second control storage unit stores a microprogram for

the IDCT and a microprogram for transferring a video block on which the IDCT has been performed to the second buffer, and

wherein the execution unit executes a processing to transfer the video block on which the IDCT has been performed to the second buffer and the IQ processing of a next video block in parallel, and executes the IDCT processing of the next video block, on which the IQ processing has been performed, using the multiplier and the adder in coordination.

122. (New) The media processing apparatus of Claim 121,

wherein the blending unit further generates a differential block representing a differential image from

video data which is to be compressed;

wherein the second buffer stores the generated differential block,

wherein the first control storage unit further stores a microprogram for discrete cosine transformation (abbreviated as the "DCT" hereafter) and a microprogram for quantization processing (abbreviated as the "Q processing" hereafter), wherein the second control storage unit further stores a microprogram for the DCT and a microprogram for transferring the video block on which the DCT has been performed to the first buffer,

wherein the execution unit further executes the DCT and Q processing on the differential block stored in the second buffer and transfers the differential block on which the DCT and Q processing has been performed to the first buffer,

wherein the data translation unit further performs variable length coding (abbreviated as the "TLC" hereafter) on the block stored in the first buffer, and

wherein the sequential processing unit further assigns header information to a block on which the VLD has been performed by the data translation unit.

123. (New) The media processing apparatus of Claim 118,

wherein the calculation unit is composed of:

a first control storage unit and the second control storage unit for respectively storing a microprogram;

a first program counter for designating a first read address to the first control storage unit;

a second program counter for designating a second read address;

a selector for selecting one of the first read address and the second read address and outputting the selected address to the second control storage unit; and

a plurality of execution units for executing the IQ and IDCT in units of blocks according to control of the microprogram by the first control storage unit and the second control storage unit, each execution unit including multiplier and an adder, and

wherein each execution unit takes charge of a partial block which is divided from the block.

124. (New) The media processing apparatus of Claim 123, wherein the calculation unit is further composed of:

a plurality of address translation tables which are set corresponding to the plurality of execution units, each address translation table storing translated addresses whose order is partially changed in a predetermined address sequence;

an instruction register group including a plurality of registers which each store a microinstruction associated with one of the translated addresses, each microinstruction forming part of a microprogram that realizes a predetermined calculation; and

a switching unit, which is set between the first and second control storage units and the plurality of execution units, for outputting microinstructions from the instruction registers to the plurality of execution units in place of a microinstruction outputted from one of the first control storage unit and the selector to every execution unit, and

wherein when the first read address or the second read address is an address of the predetermined address sequence, the address is translated into the translated addresses by the address translation tables, and

wherein the instruction register group outputs the microinstructions corresponding to the translated addresses outputted from the address translation tables.

125. (New) The media processing apparatus of Claim 124, wherein

when a microinstruction indicating one of an addition or subtraction operation is outputted from one of the instruction registers, each address translation table outputs a flag showing whether the microinstruction indicates an addition or a subtraction while the first program counter is outputting the first read address in the predetermined address sequence, the plurality of execution units perform addition or

subtraction in accordance with the flag, and

the flag is set in accordance with the microinstruction of the second control storage unit.

126. (New) The media processing apparatus of Claim 124,

wherein the second control storage unit further outputs information showing a storage destination of a microinstruction execution result at a same time of an output of the microinstruction stored in the register while the first program counter outputs the first read address of the predetermined address sequence, and

wherein each execution unit stores the execution result in accordance with the storage destination information.